REMARKS/ARGUMENTS

Reconsideration is requested in view of the following remarks. Claims 26 and 28 have been editorially revised. Support for the revisions is found in paragraph [0018] of the specification and Figures 2 and 3, among other places. Claims 26, 28 and 29 remain under consideration in the present application.

Notice Re Change of Examiner and A.U. Number

Applicant notes the change in Examiner, and A.U. number from 2828 to 2815.

Objection to the March 14, 2007 Amendment-New Matter

The amendment filed on 3/14/2007 is objected to under 35 U.S.C. §132(2) as introducing new matter into the disclosure of the invention by way of amending claims 26 and 28. Claims 26 and 28 have been editorially revised to remove any new matter. This objection is therefore overcome and should be withdrawn.

Objections to the Drawings

The drawings are objected to as not showing the new matter added by way of claims 26 and 28. Claims 26 and 28 have been editorially revised to remove any new matter, rendering this objection moot. This objection should be withdrawn.

Objection to the Specification

The specification is objected to as failing to provide proper antecedent basis for the subject matter in claims 26-29. Claims 26 and 28 have been editorially revised to remove any new matter, rendering this objection moot. This objection should therefore be withdrawn.

The specification is objected to under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 26 and 28 have been editorially revised to remove any new matter, rendering this objection moot. This objection should be withdrawn.

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Claims Rejections – 35 U.S.C. §112

Claims 26, 28 and 29 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 26 and 28 have been editorially revised to remove any new matter. This rejection is therefore overcome.

Claims 26, 28 and 29 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 26 and 28 have been editorially revised to remove any new matter. This rejection is therefore overcome.

Claims 26, 28 and 29 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 26 and 28 have been editorially revised to remove any new matter. This rejection is therefore overcome.

Claim Rejections – 35 USC §103

Claims 26, 28 and 29 are rejected under 35 U.S.C. §103(a) as unpatentable over Baird (US 4,661,726). Applicant respectfully traverses this rejection.

The invention of Baird is directed to a temperature compensation system for semiconductor logic gates where the temperature compensation is accomplished by two depletion mode FET's in electrical series relationship. The theory of operation disclosed by Baird is therefore directed solely to temperature compensation.

In contradistinction, the claimed invention is directed solely to a buffered field effect transistor logic (BFL) level-shifting/inverter circuit. The theory of operation of the invention of Baird thus bears no resemblance to the theory of operation of the claimed invention.

The claimed invention as claimed in claims 26 and 28 requires two output nodes to achieve the claimed level-shifting. The invention of Baird discloses only a single temperature compensated output node.

The rejection asserts that a voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34 of Baird's Figure 4. The invention of Baird however, has only one temperature compensated output node; and any additional output node connection between elements 33 and 34 would not be temperature compensated. Thus, if the invention of Baird were modified as suggested by the rejection, the result would be one temperature compensated output node and one additional output node that is not temperature compensated, thus defeating the purpose of the Baird invention. Therefore, no motivation exists to modify the invention of Baird to arrive at the claimed invention without improperly using the claimed invention as a template.

Baird nowhere discloses or teaches the claimed buffered field effect transistor logic (BFL) level-shifting/inverter circuit having two output nodes in which one output node is configured to transmit a signal that is level shifted from the other output node signal because the theory of operation of the Baird invention is directed solely to a single temperature compensated output node that bears absolutely no resemblance to the claimed invention. The only motivation for modifying the invention of Baird is the claimed invention itself which is not a proper basis to so modify the invention of Baird.

More specifically, the invention of Baird employs a temperature compensation circuit between the top transistor 32 and the bottom transistor 37 of a BFL circuit; while the claimed invention employs a level-shifting circuit between the top and bottom transistors, Q3 and Q4, of a BFL circuit. Modifying the invention of Baird to create two output nodes that are level-shifted from one another would undesirably result in a more complex invention having even more temperature compensation transistors in order to preserve the temperature compensation characteristics of Baird. There is simply no motivation whatsoever to modify the invention of Baird without improperly using the claimed invention as a template.

Further, since the invention of Baird is directed to a temperature compensation system, and not a BFL circuit, the invention of Baird is shown in one embodiment as a portion of a conventional BFL Schottky diode FET BFL circuit. Nowhere does Baird suggest or teach a BFL level-shifting/inverter circuit comprising solely NMOS depletion mode based devices as required by the claimed invention.

For at least these reasons, claims 26 and 28 are patentable over Baird. Claim 29 is also patentable over Baird since it depends from claim 28 that is allowable. Applicant does not concede the correctness of the rejection.

Claim Rejections – 35 USC §103

Claims 28 and 29 are rejected under 35 U.S.C. §103(a) as unpatentable over Baird in view of Tohyama (US 4,810,907) and Alok (US 6,559,068). Applicant respectfully traverses this rejection for at least the same reasons discussed above regarding the rejection of claims 26, 28 and 29.

Further, the rejection incorrectly asserts that the invention of Baird includes the BFL of Figure 4. The invention of Baird has nothing whatsoever to do with a BFL circuit, but is directed solely to a claimed temperature compensated logic gate. Although Baird does exemplify use of his temperature compensated logic gate in a Schottky diode FET BFL circuit, the disclosed Schottky diode FET BFL circuit bears no resemblance to the claimed BFL level-shifting/inverter circuit comprising solely NMOS depletion mode based devices.

For at least these reasons, claims 28 and 29 are patentable over Baird, alone or in combination with Tohyama and Alok. Neither Tohyama alone or in combination with Alok remedy the deficiencies of Baird. Applicant does not concede the correctness of the rejections or the relevance of Tohyama and Alok to the remaining claim features.

Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at (507) 351-4450.

Respectfully submitted,

Dated: September 19, 2007

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